



Jordan University of Science and Technology
Faculty of Computer & Information Technology
Computer Engineering Department

CPE236 Digital Logic Design
Summer Semester 2020-2021

Course Catalog
3 Credit Hours. Binary systems; Boolean algebra and logic gates; Simplification of Boolean functions; Combinational logic; Design of combinational logic with MSI, LSI, programmable logic devices, and hierarchical logic design; Sequential logic; Registers, counters, and memory units; Computer-aided design and logic simulation.

Text Book	
Title	Digital Design
Author(s)	M. Morris Mano and Michael D. Ciletti
Edition	5th Edition
Short Name	Ref #1
Other Information	

Course References

Short name	Book name	Author(s)	Edition	Other Information
Ref #2	Digital Design: Principles and Practices	John F. Wakerly	4th Edition	
Ref #3	Computer Engineering Hardware Design	M. Morris Mano	1st Edition	
Ref #4	Fundamentals of Logic Design	Charles Roth, Jr., Brooks Cole.	7th Edition	

Instructor	
Name	Prof. Abdel Rauf Rjoub
Office Location	E1-L3
Office Hours	

Email	abdoul@just.edu.jo
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Class Schedule & Room
Section 1: Lecture Time: Sun, Mon, Tue, Wed : 10:00 - 11:30 Room: 150 منصة الكترونية

Tentative List of Topics Covered		
Weeks	Topic	References
Weeks 1, 2, 3	Binary Systems	Ch.1 in textbook From Ref #1
Weeks 4, 5	Boolean Algebra and Logic Gates	Ch.2 in textbook From Ref #1
Weeks 6, 7	Gate-Level Minimization	Ch.3 in textbook From Ref #1
Weeks 8, 9, 10	Combinational Logic	Ch.4 in textbook From Ref #1
Weeks 11, 12, 13	Sequential Circuits	Ch. 5 in textbook From Ref #1

Mapping of Course Outcomes to Program Student Outcomes	Course Outcome Weight (Out of 100%)	Assessment method
Ability to work with different number systems; representation, conversions, and arithmetic. [1SO1]	20%	
An ability to use switching algebra theorems to solve problems. [1SO1]	15%	
An ability to use various techniques to optimize logic realization. [1SO1, 1SO2, 1SO6]	20%	
An ability to design components for combinational and sequential logic circuits; adder/subtractor, multiplier, magnitude comparator, decoders/encoders, multiplexer/demultiplexer, latch, flip-flop. [1SO1, 1SO2, 1SO6]	30%	
An ability to analyze combinational and sequential logic circuits for various applications; registers, counter, etc. [1SO1, 1SO2, 1SO6]	15%	

Relationship to Program Student Outcomes (Out of 100%)																	
A	B	C	D	E	F	G	H	I	J	K	SO1	SO2	SO3	SO4	SO5	SO6	SO7
											56.67	21.67				21.67	

Evaluation	
Assessment Tool	Weight
Mid Exam, CPE 236	30%
Final Exam	50%

quizzes	20%
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Policy	
Exams	May include: analysis, design, operation tracing, problem solving, and descriptive formats, Use your own tools only: pens ...etc, No calculators will be allowed, Instructions on the first page of the exam are very important, and Not abiding by the rules is a reason for dismissal from the exam.
Makeup Exams	Makeup exams are not given unless there is a valid excuse accepted by the dean submitted within 2 weeks of the missed exam's date.
Drop Date	Check the Records and Registration office.
Cheating	Standard JUST policy will be applied. If your cell phone is found not to be turned off during the exam, you will be suspected of attempting to cheat.
Attendance	-Excellent attendance is expected. -JUST policy requires the faculty member to assign a ZERO (35%) if a student misses 10% of the classes without an acceptable excuse accepted by the dean. -Attendance will be taken by calling names or by passing around an attendance sheet. -If you miss a class, it is your responsibility to find out about any announcements or material you may have missed.
Workload	Average work-load student should expect to spend 8 hours/week on the course (excluding lecture time)
Graded Exams and Quizzes	Graded exam papers and quizzes will be returned within a week.
Participation	-Participation in the class will positively affect your performance. -Disruption and side talks will possibly result in dismissal from class. -Turn off your cell phone before you come to class.

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