Jordan University of Science and Technology

Faculty of Computer & Information Technology

Computer Engineering Department

CPE421 Digital Integrated Circuits - JNQF Level: 6

First Semester 2024-2025

Course Catalog
3 Credit Hours. Analysis and design of CMOS digital integrated circuits, CMOS logic circuits, layout, and fabrication, MOS transistor theory, modeling MOS devices using equations and SPICE, voltage transfer characteristics, noise margins delay estimation, logical effort, electrical effort, CMOS logic circuits families: static CMOS logic, pseudo-nMOS logic, dynamic/domino logic, pass transistor logic. Latches and flip-flops, buffers and I/O circuits. semiconductor memories: DRAM, SRAM, ROM, introducing VLSI concepts. A set of laboratory experiments will provide hands-on experience.
Teaching Method: On Campus

Text Book	
Title	CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition).
Author(s)	Neil Weste, David Harris
Edition	4th Edition
Short Name	CMOS VLSI Design
Other Information	

Course References

Short name	Book name	Author(s)	Edition	Other Information
DIC	Digital Integrated Circuit: A design perspective?	J.M. Rabaey,	4th Edition	
CMOS	CMOS Digital Integrated Circuits	S.M. Kang and Y. Leblebici,	2nd Edition	

Instructor	
Name	**Prof. Abdel Rauf Rjoub**
Office Location	E1-L3

Office Hours	Sun : 08:30 - 11:30 Mon : 08:30 - 09:30 Tue : 08:00 - 10:00 Wed : 08:00 - 09:45
Email	abdoul@just.edu.jo

Class Schedule & Room
Section 1: Lecture Time: Mon, Wed : 10:00 - 11:30 Room: E2117

Prerequisites		
Line Number	**Course Name**	**Prerequisite Type**
1712310	CPE231 Digital Logic Design	Prerequisite / Study
243213	EE321 Fundamentals Of Electronics (Non Ee Students)	Prerequisite / Study

Tentative List of Topics Covered		
Weeks	**Topic**	**References**
Week 1	Design Tools and Flows, VLSIDesign: History: the past, current and future.	From **CMOS**
Week 1	CMOS Process and layout, CMOS Devices: SPICE and deep sub-micron issues.	From **CMOS**
Week 2	CMOS Inverter, Logic Operation and Design, Static CMOS Logic Gates	From **CMOS**
Week 2	Multiplexer design and Demo, D FF and Latches, Master Slave D FFs	From **CMOS**
Week 3	Fabrication Process - Part I	From **DIC**
Week 4	Circuit Characterization and Performance Estimation, Introduction	From **CMOS**
Week 4	Delay Time (Rise/Fall)	From **CMOS**
Week 5	Delay Time over long line interconnections	From **CMOS**
Week 5	Power Dissipation: Dynamic	From **CMOS**
Week 6	Power Dissipation: Static	From **CMOS**
Week 7	Power Dissipation: Leakage.	From **CMOS**
Week 8	Euler Path and Layout Design	From **CMOS**
Week 9	Design of Logic Gates.	From **CMOS**
Week 9	Rise/Fall Time Overview.	From **CMOS**
Week 10	Rise/Fall time in CMOS inverter	From **CMOS**
Week 11	Rise/Fall time over CMOS Logic Gates	From **CMOS**
Week 12	Delay Time overview	From **CMOS**

Week 13	Dynamic Logic Gates	From **CMOS**
Week 13	Static Logic Gates	From **CMOS**
Week 14	Domino Logic Gates	From **CMOS**
Week 15	Dynamic Logic Gates	From **CMOS**
Week 16	CPL Logic Gates	From **CMOS**
Week 16	Pseudo, Dual Rail, CVSL Logic Gates.	From **CMOS**

Mapping of Course Outcomes to Program Outcomes and NQF Outcomes	**Course Outcome Weight (Out of 100%)**	**Assessment method**
Students are introduced to CMOS technology modeling and use knowledge of mathematical differential equations to extract the mode of operations. [1SO1] [20A, 1SO7] [5L6K1, 5L6K2, 5L6S1, 5L6C3]	20%	
A major focus of the course is to teach students how to design and simulate basic CMOS circuits. Therefore, students are able to characterize the CMOS circuit and conduct basic CMOS experiment with proper analysis. [1SO1, 1SO6] [1SO2] [10L6S1, 5L6C4]	15%	
Students are further learn to carry the CMOS design into layout structure for further data analysis and be able to deduce the right decision on circuit design. [1SO1, 1SO6, 1SO7] [1SO2] [10L6S1, 5L6S2]	15%	
Students are challenged with engineering circuit design problems that need to meet certain CMOS circuit performances from top-to-down analysis, wherein students are familiar to identify and formulate the appropriate CMOS circuit design that meet the objective performances. [1SO1, 1SO6] [1SO1, 1SO6] [5L6C1, 5L6C2, 5L6C3]	10%	
Students need to be able to function effectively on a team, and be able to divide their design into small components? modules and distribute the tasks among each other. Finally, students learn how to integrate their accomplished tasks into complete functional real-life design that meat certain objectives. [1SO5, 1SO6] [1SO5, 1SO6] [5L6S1, 5L6C1]	10%	
Students learn to use several EDA tools related to Synopsys and Cadence. The students use schematic capture, layout tools, Spice and simulation viewer, and Synthesis tools in order to accomplish their project and labs and be able to extract and interpret data against given objectives [1SO5, 1SO6] [1SO3, 1SO5, 1SO6] [5L6S1, 5L6S2, 5L6C1, 5L6C4]	20%	
Students are familiarized with different technologies standards and their impact on design performances; thus, students get aware of contemporary issues in the filed computer circuit design. [1SO5, 1SO6, 1SO7] [1SO5, 1SO6, 1SO7] [5L6C3, 5L6C4]	10%	

Relationship to Program Student Outcomes (Out of 100%)																
A	B	C	D	E	F	G	H	I	J	K	SO1	SO2	SO3	SO4	SO5	SO6	SO7
19.05											5	30	6.67		15	20	4.29

Relationship to NQF Outcomes (Out of 100%)							
L6K1	L6K2	L6S1	L6S2	L6C1	L6C2	L6C3	L6C4
5	5	35	10	13.33	3.33	13.33	15

Evaluation	
Assessment Tool	**Weight**
First Exam	20%
Contribution	15%
Final Exam	40%
Second	25%

Policy	
Attendance	Excellent attendance is expected. In accordance with university regulations, students missing more than 20% of total classes are subject to failure. No excuses will be accepted. If you miss class, it is your responsibility to find out about any announcements or assignments you may have missed. Attendance will be recorded at the beginning or end of each class.
Participation	You are expected to participate in class. Participation includes asking and answering questions, raising issues, and suggesting solutions to the discussed problems.
Activities	Students are expected to work on activity within a group of 3-4 students. The activity could be a small software project, or a case study of a healthcare provider.
Exams	All exams will be CLOSE-BOOK. The format for the exams is generally as follows: multiple-choice, and short essay questions.
Makeup exams	The makeup exams should not be given unless there is a valid excuse. Arrangements to take an exam at a time different than the one scheduled MUST be made prior to the scheduled exam time. In accordance with university regulations, students should bring a valid excuse authenticated through valid channels in JUST.
Workload	The average work-load student should expect to spend is 6 hours/week.
Code of Conduct	Quizzes and exams need to be done individually. Copying of another student's work, even if changes are subsequently made, is inappropriate, and such work will not be accepted. Cheating or copying from neighbors on the exam is an illegal and unethical activity and standard JUST policy will be applied. All graded assignments must be your own work.

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