Jordan University of Science and Technology

Faculty of Computer & Information Technology

Computer Engineering Department

CPE454 Interfacing Lab - JNQF Level: 7

First Semester 2024-2025

Course Catalog
1 Credit Hours. 1 Credit Hours. Design and implementation of several interfacing tasks; interfacing with simple I/O devices using latches, buffers, and parallel adapters; parallel and serial interfacing to printers, scanners, and CRTs. Timer programming (wave generation, frequency meters, and real time clocks); A/D and D/A converters and data acquisition; host-to-host communication through parallel and serial links and Modems; interfacing sound chips and control circuits.
Teaching Method: On Campus

Text Book	
Title	PIC18F23K22
Author(s)	-
Edition	1st Edition
Short Name	Ref#1
Other Information	

Course References

Short name	Book name	Author(s)	Edition	Other Information
Ref#2	PIC 18 Family Data sheet	-	1st Edition	
Ref#3	Xilinx and Altera FPGA manuals	-	1st Edition	
Ref#4	NEXYS3 manual	-	1st Edition	

Instructor	
Name	**Prof. Muhannad Quwaider**
Office Location	C5-L2
Office Hours	
Email	mqquwaider@just.edu.jo

Class Schedule & Room
Section 1: Lecture Time: Tue : 13:30 - 16:30 Room: CPE01-E3L1 Section 2: Lecture Time: Thu : 13:30 - 16:30 Room: CPE01-E3L1

Prerequisites		
Line Number	**Course Name**	**Prerequisite Type**
1713541	CPE354 Microprocessor Systems Lab	Prerequisite / Pass
1714512	CPE451 Introduction To Embedded Systems	Prerequisite / Study

Tentative List of Topics Covered		
Weeks	**Topic**	**References**
Week 1	Introduction and teams	
Week 2	Introduction to PIC microcontroller programming	
Week 3	PIC Applications (Switches, LEDs, Buzzer and 7-segments display)	
Week 4	PIC Applications (LCD and ADC)	
Week 5	PIC Applications (Motor)	
Week 6	PIC Applications (Interrupt experiments)	
Week 7	Midterm Exam	
Week 8	Introduction to Verilog HDL + Using ISE 14.6 software to program NEXYS3	
Week 9	Use Verilog to implement Combinational Circuits	
Week 10	Use Verilog to implement Sequential Circuits (Part 1)	
Week 11	Use Verilog to implement Sequential Circuits (Part 2) + Display on multiple 7-segments displays	
Week 12	Review	
Week 13	Final Exam	

Mapping of Course Outcomes to Program Outcomes and NQF Outcomes	Course Outcome Weight (Out of 100%)	Assessment method

The ability to program a microcontroller/FPGA and interface it with different components to solve engineering problems [1SO1] [1L7K1]	45%	
The ability to conduct different experiments using a microcontroller/FPGA and connected components to assess the implemented solution for the engineering problem in question. This involves data collection, analysis, and interpretation [1SO5] [1L7C1]	10%	
The ability to work effectively within a team and demonstrate leadership and collaboration skills during the laboratory experiments using a microcontroller/FPGA connected with different components. This involves identifying experiment goals as well as planning and executing the tasks. [1SO6] [1L7S3]	45%	

Relationship to Program Student Outcomes (Out of 100%)																	
A	B	C	D	E	F	G	H	I	J	K	SO1	SO2	SO3	SO4	SO5	SO6	SO7
											45				10	45	

Relationship to NQF Outcomes (Out of 100%)		
L7K1	L7S3	L7C1
45	45	10

Evaluation	
Assessment Tool	**Weight**
Semester works	40%
Final Exam	40%
Mid Exam	20%

Policy	
Attendance	Excellent attendance is expected. In accordance with university regulations, students missing more than 20% of total classes are subject to failure. No excuses will be accepted. If you miss class, it is your responsibility to find out about any announcements or assignments you may have missed. Attendance will be recorded at the beginning or end of each class.
Participation	You are expected to participate in class. Participation includes asking and answering questions, raising issues, and suggesting solutions to the discussed problems.
Activity	Students are expected to work on an activity within a group of 3-4 students. The activity could be a small software project, or a case study of a healthcare provider.
Exams	All exams will be CLOSE-BOOK. The format for the exams is generally as follows: multiple-choice, and short essay questions.

Makeups	Makeup exam should not be given unless there is a valid excuse. Arrangements to take an exam at a time different than the one scheduled MUST be made prior to the scheduled exam time. In accordance with university regulations, students should bring a valid excuse authenticated through valid channels in JUST.
Workload	Average work-load student should expect to spend is 6 hours/week
Code of Conduct	Quizzes and exams need to be done individually. Copying of another student's work, even if changes are subsequently made, is inappropriate, and such work will not be accepted. Cheating or copying from neighbor on exam is an illegal and unethical activity and standard JUST policy will be applied. All graded assignments must be your own work.

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