Jordan University of Science and Technology

Faculty of Computer & Information Technology

Computer Engineering Department

CPE748 Vlsi Design - JNQF Level: 6

First Semester 2024-2025

Course Catalog
3 Credit Hours. The VLSI Design Course for the master level emphasizes continuing basic knowledge and increasing the background on the basic and modern topics of recent technology factors. It will cover the theories and techniques of digital VLSI design in CMOS technology. In this course, we will study the fundamental concepts and structures of designing digital VLSI systems including CMOS devices and circuits, standard CMOS fabrication processes, CMOS design rules, static and dynamic, logic structures, interconnect analysis, CMOS chip layout, simulation and testing, low power techniques, design tools and methodologies, VLSI architecture. Students in this course will run and simulate assignments based on project orientation. Simulation tools like Mathematica, Matlab, and SPICE Simulations are expected to run for extracting models for the above topics.
Teaching Method: On Campus

Text Book	
Title	CMOS VLSI Design: A Circuits and Systems Perspective, 3rd ed, Addison Wesley, 2005.
Author(s)	Weste & Harris,
Edition	3rd Edition
Short Name	VLSI Design
Other Information	

Course References

Short name	Book name	Author(s)	Edition	Other Information
Reference 1	Digital Integrated Circuit: A design perspective	J.M. Rabaey,	4th Edition	
Reference 2	CMOS Digital Integrated Circuits	Sung-Mo Kang, Yusuf Leblebici.	3rd Edition	

Instructor	
Name	**Prof. Abdel Rauf Rjoub**

Office Location	E1-L3
Office Hours	Sun : 08:30 - 11:30 Mon : 08:30 - 09:30 Tue : 08:00 - 10:00 Wed : 08:00 - 09:45
Email	abdoul@just.edu.jo

Class Schedule & Room
Section 1: Lecture Time: Wed : 13:00 - 16:00 Room: C2007

Tentative List of Topics Covered		
Weeks	**Topic**	**References**
Week 1	An introduction to CMOS basics	
Week 2	An introduction to CMOS basics	
Week 3	MOS Transistor Theory - Solid State.	
Week 4	MOS Transistor Theory - Modeling and Simulation	
Week 5	CMOS Processing Technology & Design Rules	
Week 6	Fundamental Logic Gates, Rules, Guidelines.	
Week 7	Circuit Characterization and Performance Estimation - Delay Estimation, Logical Effort & Transistor Sizing.	
Week 8	Circuit Characterization and Performance Estimation - Power Dissipation.	
Week 9	Circuit Characterization and Performance Estimation - Interconnect, Wire Engineering, Design Margin, Reliability and Scaling	
Week 10	Circuit Characterization and Performance Estimation Design Margin, Reliability and Scaling	
Week 11	Circuit Simulation.	
Week 12	Assignments Project Based on.	
Week 13	Assignments Project Based on.	

Week 14	Assignments Project Based on.	

Mapping of Course Outcomes to Program Outcomes and NQF Outcomes	Course Outcome Weight (Out of 100%)	Assessment method
Design a logic function using the CMOS design style. [5A, 5B] [5L6K1]	10%	
Draw the stick diagram, a transistor-level schematic for logic circuits. [2C, 3D] [2L6K1, 3L6K2]	5%	
Apply the I-V equations. [5A, 5B, 5E] [5L6S3, 5L6C1, 5L6C2]	15%	
Examine the non-ideal I-V effects (e.g. body effect, velocity saturation, sub-threshold conduction, etc.) and other VLSI circuit design issues. [5G, 5H] [5L6C2, 5L6C3]	10%	
Analyze circuit design models and techniques, such as the RC delay model, Elmore delay model, and parasitic delay model. [5H, 5I, 3SO4, 2SO5] [5L6S3, 5L6C1, 5L6C2]	15%	
Calculate transistor parameters, gate parameters, circuit parameters, IC chip power consumption, logical effort and other IC chip parameters. [5SO4, 5SO6] [5L6C2, 5L6C3]	10%	
Use interconnects in circuit design. [5SO6, 5SO7]	10%	
Prepare SPICE simulation. [5SO7] [5L6C3]	5%	
Assignment Project Evaluation. [2A, 2B, 2C, 5D, 2E, 3F, 2G, 2SO2] [2L6K1, 2L6K2, 2L6S1, 2L6S2, 2L6S3, 2L6C1, 2L6C2, 2L6C3, 2L6C4, 2L6C5]	20%	

Relationship to Program Student Outcomes (Out of 100%)																	
A	B	C	D	E	F	G	H	I	J	K	SO1	SO2	SO3	SO4	SO5	SO6	SO7
12	12	4	8	7	3	7	10	5				2		8	2	10	10

Relationship to NQF Outcomes (Out of 100%)									
L6K1	L6K2	L6S1	L6S2	L6S3	L6C1	L6C2	L6C3	L6C4	L6C5
14	5	2	2	12	12	22	17	2	2

Policy	
Attendance	- It is expected that the students attend all classes, in case of any unexpected matter, students should send an email or apology before the same day next week.
Assignments:	- It is expected to complete the assignments due time, no delay will be given to submit the assignments after the deadline.
Exams, homeworks, and Assignments.	- It is expected that the students to be ready to write several exams, do different homework, and run different mathematical models based on different simulation tools and CAD orientation.

JUST Roles and Guidlines	For any unexpected case including cheating, absence from the exams, and so on, the rules and guidelines will be applied in that case.

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