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Drain Induced Barrier Lowering (DIBL) Accurate Model for Nanoscale Si-MOSFET Transistor

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Abstract: In this paper, an accurate new model for drain induced barrier lowering (DIBL) tunneling in silicon on insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) is proposed. The effect of drain (Vds) and substrate (Vbs) voltages variation on DIBL is discussed. The dependency of channel length variation (?L), junction depth (rj), and substrate impurity concentration (NB) on DIBL is analyzed, and new equations are obtained. The evaluation results for the proposed model using MATHEMATICA give good agreement when compared with analytical and simulation results for BSIM4 level 54 and recent well-known models using HSPICE simulator.