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Modeling in Nanoscale CMOS technology: Challenges and Design Requirements

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Abstract: In this paper, recent modeling techniques of Compact Metal Oxide Semiconductor (CMOS) transistor are presented and analysed in details. The challenges of modeling in Nanoscale technology with efficient solutions are also analyzed. The effect of some Nanoscale effective parameters on the characteristic (I-V) function are explained: Subthreshold leakage (Isub), Gate Leakage (Ig), Band-to-Band Tunnelling (IBTBT) are introduced with some recommendations about how it can be minimized. The simulation results show that the professional model is that one with high accuracy and low processing delay.