Jordan University of Science and Technology

High performance FPGA-based decimal-to-binary conversion schemes for decimal arithmetic

Authors: Osama Al-Khaleel, Zakaria Al-Qudah, Mohammad Al-Khaleel , Christos Papachristou

Abstract: Despite that it has been recognized that decimal arithmetic is more suitable than binary arithmetic for human-centric applications, binary arithmetic is still predominant in today?s computers. One approach to bridging this gap involves converting the decimal operands to binary, performing arithmetic in binary, and converting the result back to decimal. Based on this approach, this paper presents novel high-performance decimal-to-binary conversion circuits to support decimal arithmetic over different FPGAs families. Our circuits are based on a simple, yet effective idea. Bits of the BCD inputs are grouped into a number of groups. The contribution of each group to the overall binary result is computed separately. Then these contributions are added to form the final binary result. The performance evaluation presented in this paper indicates that the proposed circuits perform significantly better than existing BCD-to-binary conversion circuits. Furthermore, for a given FPGA family, the comparison reveals that certain bit-grouping may perform better than others. In addition, we have studied the growth in area and time for each bitgrouping scheme with respect to the number of digits in the BCD input.