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Fast Binary/Decimal Adder/Subtractor with a Novel Correction-Free BCD Addition

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Abstract: This paper proposes a novel architecture for high speed combined binary/decimal addition/subtraction. We start by designing a correction-free Binary Coded Decimal (BCD) digit adder which exhibits high performance. We then use the proposed BCD digit adder to create a fast multi-digit BCD adder. The resulting multi-digit BCD adder is then used to build a combined binary/decimal addition/subtraction unit. The proposed combined binary/decimal addition/subtraction unit has been functionally verified and then implemented on Xilinx FPGA using Xilinx CAD tools. Implementation results show that our design outperforms the existing designs in terms of speed and most of the existing designs in terms of area.