Dr. KHALDOON MHAIDAT

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Education

- Ph.D. in electrical and computer engineering, Oregon Graduate Institute/OHSU, Portland, Oregon, USA, 2006, Thesis: Representations and Circuits for Time Based Computation. Semiconductor Research Corporation (SRC) sponsored research.
- M.S. in electrical and computer engineering, Oregon State University, Corvallis, Oregon, USA, 2002, Thesis: Prototyping a Scalable Montgomery Multiplier using Field Programmable Gate Arrays (FPGAs).
- B.S. in electrical and computer engineering, Jordan University of Science and Technology, Irbid, Jordan, 1999, Dean's honor list, Rank=7 out of 102.

Experience

- 9/2006-Now: Assistant professor, computer engineering department, JUST, Irbid, Jordan.
- 9/2011-9/2012: Chairman of the computer engineering department, JUST, Irbid, Jordan.
- 9/2010-5/2013: Adjunct assistant professor, New York Institute of Technology (NYIT), Amman, Jordan.
- 3/2006-9/2006(Resigned): Component Design Engineer, Desktop Platform Group, Intel, Santa Clara, California.
- 2/2005-9/2005: Graduate technical Intern (Speed path & micro-architecture validation), Desktop Platform Group, Intel, Santa Clara, California.
- 6/2004-11/2004: Graduate technical Intern (Mixed signal validation), Logic Technology Development, Microprocessor Design Group, Intel, Hillsboro, Oregon.
- 6/2003-1/2004: Graduate technical Intern (DFT & post-Silicon validation), Logic Technology Development, Microprocessor Design Group, Intel, Hillsboro, Oregon.
- 6/2002-3/2006: Research Assistant, ECE, OGI/OHSU, Beaverton, Oregon.
- 9/2000-6/2002: Research Assistant, ECE, Oregon State University, Corvallis, Oregon.
- 9/2001-12/2001: Teaching Assistant, ECE, Oregon State University, Corvallis, Oregon.
- 10/1999-7/2000: Teaching Assistant, Computer Engineering, Yarmouk University, Jordan.
- 7/1999-10/1999: Programmer, Arabia.On.Line, Amman, Jordan.
- 7/1998-9/1998: Intern, Institut für Telematik, Trier, Germany.

Awards, Scholarships, Fellowships, Grants, and Donations

- IEEE Computer Society TTTC Continuous Service Award in recognition of 10 years continuous service for IEEE International Design & Test Symposium.
- IBM Faculty Award for the project entitled "Performance and power analysis of hypervisor based power management in many-core systems" ($7000).
- Best paper award for the paper: "FPGA-Based Features Extraction Unit for Arabic Characters," in the 4th International Conference on Information and Communication Systems, Irbid, Jordan, 2013.
- Mentor, 3rd prize in the 5th international microelectronics Olympiad.
- Intel Prescott (P4 90nm) achievements award

- Intel Cedarmill (P4 65nm) achievements award
- Intel kudos award for writing an automation script for speed-path debug which was critical to timely project completion in Cerdarmill P4 CPU
- Semiconductor Research Corporation (SRC) Ph.D. Fellowship.
- IAESTE-DAAD engineering internship awarded for top engineering students.
- Ministry of Higher Education scholarship, 5-year for B.S. study.
- JUST scholarship, 5-year for M.S. and Ph.D. study.
- Engineering Dean's honor list.
- Silego GreenPAK2 power supply design project fund ($8000).
- Silego GreenPAK2 and GreepPAK3 programmable mixed-signal IC design evaluation kits.
- Cypress PSoC3 and PSoC5 development kits
- Synopsys full North-America university full bundle (2-year 20-user license, $20M+ industry value) + membership and full access to Synopsys university program.
- Xilinx ISE full system edition (75-user license) + membership and full access to Xilinx university program.
- SUN Sparc T2 server (~$12000) + membership and full access to SUN university program.
- Four Virtex-5 FPGA prototyping boards from SUN Microsystems

Research Interests

- Electronics design and automation: VLSI, ASIC, FPGA, SoC, NoC, analog/digital/mixed-signal IC design and validation, nano-electronics, nano-technologies
- Microprocessors, microcontrollers, and embedded systems design and validation
- Information and network security: cryptography, intrusion detection
- Intelligent systems: machine vision, signal/image/video processing, pattern recognition, OCR, speech recognition, robotics, sensors
- Computer systems: hypervisors, virtualization, file systems, cloud computing, performance evaluation, power management, multi-core systems
- Wireless sensor networks

Professional Services & Memberships

- General co-chair of the 10th IEEE International Design and Test Symposium (IDT 2015)
- TPC member of the IEEE International Design and Test Symposium (IDT)
- TPC member of the International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)
- TPC member of the International Conference on Information & Communication Systems (iCICS)
- TPC member of the IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT)
- Editorial board member for the International Journal of Embedded and Real-Time Communication Systems (IJERTCS)
- Editorial board member for HSOA Journal of Nanotechnology: Nanomedicine & Nanobiotechnology
- Reviewer for the Microelectronics Journal by Elsevier
- Reviewer for the International Journal of Modeling and simulation
- Reviewer for the Journal of King Saud University - Computer and Information Sciences

- Sub-reviewer for the International Journal of Electronics
- Committee member of the international microelectronics Olympiad of Armenia organized and sponsored by Synopsys
- Active collaborator with Synopsys Armenia Educational Department (SAED) for EDA training, curriculum development, and research; received training myself and sending students for summer internships every year
- Synopsys, Xilinx, and Sun/Oracle Liaison at JUST
- Founder and supervisor of the Circuits and Systems Research Lab and group at JUST
- Supervisor/co-supervisor of the thesis work of 10+ MS students at JUST
- Thesis committee member for a number of MS students at JUST and other universities in Jordan
- Supervisor/co-supervisor of graduation projects of many BS students at JUST
- Managed the CPE department at JUST during the academic year 2011/2012.
- Graduate Studies Committee, CPE department and CIT College at JUST
- Member of the CIT College council
- Accreditation and Quality Assurance Committee, CPE department at JUST
- Curriculum Development Committee, CPE department at JUST
- Graduation projects Evaluation Committee, CPE department at JUST
- Scientific Research Committee, CPE department at JUST
- Course Schedule Committee, , CPE department at JUST
- Tenders and Labs Committee, , CPE department at JUST
- Study Plans and Courses Transfer Committee, CPE department at JUST
- Scholarships and hiring Committee, CPE department at JUST

Academic Development Training & Workshops

- Development of curriculum & study plans for Accreditation Board for Engineering and Technology (ABET)
- Modern university instructional methods
- Academic testing and evaluation
- ICT-focused business entrepreneurship by Oasis500

Technical Skills

- Electronics design, test, and automation:
    - Verilog, VHDL, Verilog-A/MS, VHDL-A/MS, SPICE
    - Intel: Opus, Presto, Lynx, iHDL, FRITS/KAVERI, MAX, ArchSim, Csim, TangoLR, Aspen, In-Target Probe (ITP) hardware & software, hands-on experience in Intel post-silicon debug labs
    - MentorGraphics: DesignArchitect, ModelSim, Eldo, AccuSimII, LeonardoSpectrum, ADMS, ICStation, Calibre
    - Xilinx: ISE, iSIM, XMD, SDK, EDK, CoreGen, BSB
    - Synopsys: VCS, Design compiler, IC compiler, Custom Designer, PrimeTime, HSPICE
    - Cadence: OrCAD/PSpice, Virtuoso
    - ExpressPCB, EAGLE PCB
    - Multi-million-dollar IMS Vanguard tester hardware & software

- Tektronix, HP, Agilent, & Fluke digital oscilloscopes & logic analyzers

- Programming and scripting:
  - C#.NET, C/C++, Perl, Java, Fortran
  - CGI, SQL, HTML, CSS, JavaScript, PHP
  - Assembly: Intel, Motorola, ARM, MIPS, RISC
  - MATLAB, Maple
- Operating systems:
  - UNIX, Linux, MS-DOS, Windows

Projects and Assignments

- Representations & circuits for inter-pulse-interval (IPI) based computation & conversion: design, simulation, semi-custom layout, LVS & DRC verification, parasitics extraction, back-annotation, post-layout simulation, fabrication, & test of a TSMC 0.35um CMOS chip. Semiconductor Research Corporation (SRC) sponsored Ph.D. research.
- Speed path debug & micro-architecture validation for Cedarmill CPU: This includes using FRITS/KAVERI to generate pseudo-random long tests, loading & running tests on Merlin platform, extracting the data & instruction seeds for the worst case Orphan & generating the worst case trace to be run on the structural tester for speed path debug. It also includes writing IA-32/64 assembly & MAX tests that targets certain parts of the CPU for fault grading. It also includes using the NetBatch tools to run & generate 20K+ golden traces per major Silicon stepping and debugging & fixing failures.
- Mixed signal validation for Cedarmill CPU: This includes using ADMS, Eldo, ModelSim, & Presto/Lynx for pre-silicon validation of mixed signal designs like the thermal sensor, rise & fall time control (RFTC), on-die VRM, DLLs, & PLLs.
- DFT design validation on Prescott CPU & analysis of performance parametrics from high volume manufacturing (HVM) test database: This includes using the IMS Vanguard tester & the ITP platform for post-silicon validation of DFT designs like I/O per-leg driver test (PLDT), I/O level generator (LevGen), on-die droop detector (ODDD), & DLLs.
- DC-DC buck converter circuit design using Silego's GreenPAK2 programmable mixed-signal array. Design was validated by designing and manufacturing a PCB using the ExpressPCB tool and service.
- Perl script that uses Intel unified data model (UDM) library to build the netlist of a Mega block in the Cedarmill CPU from ASPEN node reports which contain power vs. activity information. This tool was used to perform power optimization analysis.
- ITP program that automates platform-level programming & data collection of the ODDD circuit which helped in characterizing first, second, & third droops in Prescott.
- Design & simulation of an operational amplifier using TSMC 0.25um CMOS process, an operational amplifier, & a latching comparator (decision circuit & high sensitivity D flip-flop) using Maxim's GST2 bipolar process.
- ASIC implementation of a special peripheral-assisted microcontroller, which has a RISC core, a universal asynchronous receiver and transmitter (UART), a pulse width modulator (PWM), and a parallel input output port (PIO).
- ASIC-to-FPGA conversion of Montgomery multiplication based cryptographic processor.
- EPP2MM Interface circuit & driver which support EPP based communication between a PC and the Montgomery multiplication processor above residing on a D2 FPGA board.

- FPGA implementations of Montgomery multiplier.
- RISC561 machine emulator, 2-pass assembler, and direct linking loader.
- Building and testing a Motorola 68000 based computer system.
- Porting MIPS R10000 super scalar processor to Stanford SimOS machine simulator.
- Virtual memory management system simulator.
- CGI/Perl web based status report submission & tracking tool.
- CGI/Perl scripts & specialized POP3 client that interface with a large hardware verification system.
- GITEX 2000 online database using Perl & mySQL under Unix.
- Ethernet and Token-Ring networks simulation.
- Random access networks simulation: Pure Aloha, Slotted Aloha, CSMA, and CSMA/CD.

Research Publications

- Raed Bani-Hani, Salah Harb, Khaldoon Mhaidat, “Very Compact and Efficient 32-Bit AES Core Design using FPGAs for Small-Footprint Low-Power Embedded Applications," Accepted for publication in Journal of Circuits, Systems, and Computers, Jan. 20, 2016.
- E. Taqieddin, O. Abu-Rjei, K. Mhaidat, and R. Bani-Hani, “Efficient FPGA Implementation of the RC4 Stream Cipher using Block RAM and Pipelining,” the 6th International Conference on Emerging Ubiquitous Systems and Pervasive Networks (EUSPN), Berlin, Germany, 2015.
- K. Mhaidat and A. Hamzah, “A New Efficient Reduction Scheme to Implement Tree Multipliers on FPGAs,” in the 9th IEEE International Design and Test Symposium (IDT), Algiers, Algeria, 2014.
- K. Mhaidat, A. Baset, and O. Al-Khaleel, “OpenSPARC Processor Evaluation using Virtex-5 FPGA and High Performance Embedded Computing (HPEC) Benchmark Suite,” International Journal of Embedded and Real-Time Communication Systems (IJERTCS), Volume 5, Issue 1, January-March 2014.
- K. Mhaidat, M. Alali, and I. Aljarrah, “Efficient Low-Power Compact Hardware Units for Real-Time Image and Video Processing,” International Journal of Information Technology and Web Engineering (IJITWE), Volume 9, Issue 4, October-December 2014.
- M. Alali, K. Mhaidat and I. Aljarrah, “Implementing image processing algorithms in FPGA hardware,” in IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT), Amman, Jordan, 2013.
- K. Mhaidat, M. Altahat and O. Al-Khaleel, “High-Throughput Hardware Implementation of Threefish Block Cipher on FPGA," in the 4th International Conference on Information & Communication Systems (iCICS), Irbid, Jordan, 2013.
- Inad Aljarrah, Osama Al-Khaleel, Khaldoon Mhaidat, Mu'ath Alrefai, Abdullah Alzu'bi, and Mohammad Rabab'ah, “Automated System for Arabic Optical Character Recognition with Lookup Dictionary,” Journal of Emerging Technologies in Web Intelligence, Academy Publisher, Volume 4, Number 4, November 2012.
- Inad Aljarrah, Osama Al-Khaleel, Khaldoon Mhaidat, Mu'ath Alrefai, Abdullah Alzu'bi, and Mohammad Rabab'ah, “Automated System for Arabic Optical Character Recognition,” Proceedings of the 3rd International Conference on Information and Communication Systems (iCICS'12), Article No. 5, ACM, 2012.
- Osama Al-Khaleel, Inad Aljarrah, Abdelrahman Idries, and Khaldoon Mhaidat, “Hardware Implementation of Web Based Arabic Optical Character Recognition Units,” Journal of Emerging Technologies In Web Intelligence, Volume 6, Issue 2, pp.210-219, May 2014.

- O. Al-Khaleel, A. Idris, K. Mhaidat and I. Aljarrah, “FPGA-Based Features Extraction Unit for Arabic Characters," in The 4th International Conference on Information and Communication Systems, Irbid, Jordan, 2013.
- Raed Bani-Hani, Salah Harb, Khaldoon Mhaidat, Eyad Taqieddin, “High-Throughput and Area-Efficient FPGA Implementations of Data Encryption Standard (DES)," Circuits and Systems Journal, SCIRP, Vol. 5, No. 3, March 2014.
- Mohammad M. Shurman, Zaid A. Alomari, Khaldoon M. Mhaidat, “An Efficient Billing Scheme for Trusted Nodes Using Fuzzy Logic in Wireless Sensor Networks," Wireless Engineering and Technology Journal, SCIRP, Vol. 5, No. 3, July 2014.
- O. Al-Khaleel, N. Tulic and K. Mhaidat, “FPGA implementation of binary coded decimal digit adders and multipliers," in The 8th International Symposium on Mechatronics and its Applications (ISMA), 2012.
- Osama Al-Khaleel, Mohammad Al-Khaleel, Zakaria Al-Qudah, Christos A. Papachristou, Khaldoon Mhaidat, Francis G. Wolff, “Fast binary/decimal adder/subtractor with a novel correction-free BCD addition,” 18th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2011.
- K. Mhaidat, M. Jabri and D. Hammerstrom, “Representation, Methods, and Circuits for Time Based Conversion and Computation,” International Journal of Circuit Theory and Applications, Wiley, Volume 39, Issue 3, pages 299–311, March 2011.
- K. Mhaidat, M. Jabri and D. Hammerstrom, “Compact Low-Power Time-Based Conversion with Noise Immunity Similar to Digital Conversion,” Analog Integrated Circuits and Signal Processing Journal, Springer, Volume 64, Number 2, August 2010.
- K. Mhaidat, M. Jabri and D. Hammerstrom, “Compact Low-Power Time-Based Conversion with Noise Immunity Similar to Digital,” International Symposium on Signals Circuits and Systems (ISSCS), IEEE, July 2009.
- Khaldoon M. Mhaidat, Marwan Jabri, Daniel Hammerstrom, “IPI Chip Design and Test Results for Synchronous IPI Based Computation and Conversion,” Semiconductor Research Corporation (SRC) report, March 2005.
- Khaldoon M. Mhaidat, Marwan Jabri, Daniel Hammerstrom, “The Work toward an IPI Chip and VHDL-AMS Library,” SRC report, March 2004.
- Khaldoon M. Mhaidat, Marwan Jabri, Daniel Hammerstrom, “Design of IPI Based Computation Blocks with Accuracy, Performance, and Price Analysis,” SRC report, September 2003.

Invited Talks, Panels, and Presentations

- Invited talk at Khalifa University about “Algorithms and Scalable Architectures for Montgomery Modular Multiplication for Public-Key Cryptography,” Abu-Dhabi, UAE, April 13, 2016.
- Invited Panel about “Electronics Design & Test Ecosystem in MENA Region” at the 10th IEEE International Design and Test Symposium, Dead Sea, Jordan, Dec. 14-16, 2015.
- Presentation on “A New Efficient Reduction Scheme to Implement Tree Multipliers on FPGAs,” at the 9th IEEE International Design and Test Symposium (IDT), Algiers, Algeria, 2014.
- Presentation on “FPGA-Based Features Extraction Unit for Arabic Characters," at the 4th International Conference on Information and Communication Systems (iCICS), Irbid, Jordan, 2013.

- Presentation on “High-Throughput Hardware Implementation of Threefish Block Cipher on FPGA," in the 4th International Conference on Information & Communication Systems (iCICS), Irbid, Jordan, 2013.
- Presentation on “Automated System for Arabic Optical Character Recognition,” at the 3rd International Conference on Information and Communication Systems (iCICS), Irbid, Jordan, 2012.
- Presentation on “Fast binary/decimal adder/subtractor with a novel correction-free BCD addition,” at the 18th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Beirut, Lebanon, 2011.

Undergraduate Courses Taught

- Computer systems project (CPE559)
- Digital integrated circuits (CPE453/CPE420)
- Special topics in computer engineering (CPE595): Embedded systems
- Advanced digital systems design (CPE433)
- Computer design (CPE552)
- Digital logic design (CPE251/CPE231)
- Digital logic design and computer architecture for non-CPE students (CPE254)
- Digital logic design lab (CPE253)
- Computer organization and design (CPE252)
- Hardware description language (HDL) lab (CPE350)
- Microprocessor systems and assembly language (CPE351/CPE353)
- Microprocessor systems for non-CPE students (CPE353)
- Microprocessor systems design and lab (CPE451)
- Microprocessor interfacing lab (CPE452)
- Microprocessor programming lab (Oregon state university)
- Microprocessor systems design (Yarmouk university)
- Microprocessor systems design lab (Yarmouk university)
- Operating systems lab (Yarmouk university)
- Visual programming using C#.NET (SE310)

Graduate Courses Taught

- Real-time embedded systems (CPE746)
- VLSI systems (CPE748)
- Special topics in computer engineering (CPE779): CMT processors and FPGAs
- Computer Architecture II (NYIT EENG-741)
- Computer systems (NYIT EENG-660)

Examples of Graduation Projects Supervised

- Arabic optical character recognition (A-OCR) software
- CMU Sphinx Arabic speech recognition (ASR) on Linux platform
- Arabic speech recognition (ASR) on Android platform
- Plotting Robot arm
- Screw-fastening Robot

- KIVERIA: Microsoft Kinect based virtual reality
- Eye-protection screen device
- Network Intrusion detection system (NIDS)

Examples of Graduate Course Projects Supervised

- Arabic optical character recognition (A-OCR) on FPGA
- Image/video processing on FPGA
- Threefish block cipher on FPGA
- Secure Hash Algorithm SHA-256 on FPGA
- Blake, Grøstl, JH, Keccak SHA-3 algorithms on FPGA
- Lightweight Hummingbird cipher on FPGA
- DES block cipher on FPGA
- IDEA block cipher on FPGA
- RC4 stream cipher on FPGA
- Mickey , Grain , Trivium stream ciphers on FPGA
- Low-power RFID system
- ECG signal detection and classification
- Lempel-Ziv compression algorithm on FPGA
- Gray and colored medical image enhancement
- Image contrast enhancement by histogram equalization
- Karatsuba multiplication on FPGA
- Montgomery modular multiplication on FPGA

M.S. Theses Supervised

- Ahmad Baset, Title: Chip Multithreaded (CMT) Processor Validation Using Field Programmable Gate Arrays (FPGAs), 11/2010
- Yahya Flaifel, Title: Pattern Matching Hardware Implementation using Field Programmable Gate Arrays (FPGAs), 1/2013
- Mohammad Helail, Title: Analysis of File System Impact on Performance and Energy Consumption in Cloud Server Systems, 1/2014
- Salah Harb, Title: FPGA based embedded system implementation of AES algorithm, 4/2014
- Zaid Al-Omary, Title: An efficient Billing Scheme for Trusted Nodes in Wireless Sensor Networks, 5/2014
- Mohammad Altahat, Title: Study of Performance and Power Consumption of Hypervisor Systems, 6/2014
- Asma Bataineh, Title: Enhanced FPGA Implementations of the Scalable Montgomery Multiplication Algorithm, 6/2014
- Abdullah Anati, Title: Performance and Power Analysis of Hypervisors in Many-Core Systems, 11/2014
- Hiba Al-Dahoud, Title: Cryptanalysis and Improvement of Mutual Authentication Protocols in Radio Frequency Identification Systems, 12/2015
- Heba Adnan, Title: TBD, Area: WSN security protocols, in progress
- Ameera Al-Momany, Title: TBD, Area: Cryptography, in progress

References

- Prof. Dr. Marwan Jabri, Ph.D. supervisor at OGI/OHSU, CTO of Dillithium Networks, marwan@dilithiumnetworks.com
- Prof. Dr. Dan Hammerstrom, Ph.D. co-supervisor at OGI/OHSU, IEEE fellow, Professor and associate dean for research, ECE, Portland State University, strom@cecs.pdx.edu
- Prof. Alexandre Tenca, M.S. supervisor, ECE, Oregon State University, tenca@ece.orst.edu
- Prof. Dr. Çetin Kaya Koç, M.S. co-supervisor, IEEE fellow, CS, University of California, koc@cs.ucsb.edu
- Prof. Dr. Omar Al-Jarrah, Ex-vice president of JUST, President of Amman Arab University, aljarrah@just.edu.jo
- Prof. Dr. Mohammad Al-Rousan, Ex-dean of CIT college, JUST, alrousan@just.edu.jo
- Prof. Dr. Osama Al-Khaleel, Chairman of CPE department, JUST, oda@just.edu.jo
- Dr. Tawfik Arabi, Manager, Intel, IEEE fellow, tawfik.r.arabi@intel.com
- Dr. Ali Muhtaroglu, Manager, Intel, ali.muhtaroglu@intel.com
- Dr. Christopher Pan, Manager, Intel, christopher.pan@intel.com
- Jalal Yazdi, Manager, Intel, jalal.r.yazdi@intel.com
- Nazar Syed Haider, Manager, Intel, nazar.syed.haider@intel.com
- Amit Rane, Manager, Intel, amit.s.rane@intel.com
- Dr. Yervant Zorian, Chief Architect and Fellow, Synopsys, IEEE fellow, yervant.zorian@synopsys.com
- Dr. Hazem ElTahawy, Managing Director MENA Region, Mentor Graphics, hazem_eltahawy@mentor.com
- Prof. Dr. Vazgen Melikyan, Director of SEAD, Synopsys, vazgen.melikyan@synopsys.com
- John McDonald, VP, Silego, jmcdonald@silego.com
- Jeffrey Chung, Manager, Silego, jchung@silego.com