Saleh Abdel-hafeez, Associate Prof.

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http://www.just.edu.jo/FacultiesandDepartments/it/Departments/cpe/Pages/Objectives.aspx

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1. EXPERIENCES:

A. Altera.com consultant for high speed and custom FPGA I/O
1999-2002 (US, Silicon Valley)

B. Chief Scientist at Viatechnology.com in area of SRAM and ADC SAR
2000-2002 (US, Silicon Valley)

C. Senior member of technical staff at S3.com incorporated in area of Computer Graphics arithmetic AND AGP IO 1997-2000 (US, Silicon Valley)

D. Adjunct professor at Santa Clara University 1998-2002 (US, Silicon Valley)

E. Chairman of Computer Eng. Dept. at Jordan University of Science and Technology,
Sept.10, 2012 (JUST, IRBID)

F. Associate Prof. at Jordan University of Science and Technology,
Sept. 14, 2010 (JUST,IRBID)

G. Vice Dean at Jordan University of Science and Technology
Sept. 2003-2005 (JUST, IRBID)

H. Assistant Prof. at Jordan University of Science and Technology
Sept. 2003-2007 (JUST, IRBID)

2. EDUCATION:

01/93-05/97 **Ph.D**. In ASIC's design, VLSI system design, and high performance Computer architecture design.
PhD Area of research: Fuzzy logic and neural net processing algorithms. All required VLSI and VHDL chip implementation. Dissertation Title: "ASIC IMPLEMENTATION OF THE SYMMETRIC FUZZY PROCESSOR AND ITS APPLICATION TO ADAPTIVE SYSTEMS"
The University of Texas at El Paso (UTEP), El Paso, TX. 79902

01/90-08/91 **MSEE** in the area of computer architecture and vision (signal, image, speech)
New Mexico State University (NMSU), Las Cruses, NM.
Project Title: "Edge Detection Using Signal Processing Technique"

11/85-08/89 **BSEE** in the areas of electronics, communication theories, and control.
Tennessee Technological University (TTU).
Project Title: "Discrete Implementation of RISK Microprocessor Computer System"

06/1989 Engineering in Training Examination.

3. ***PUBLICATIONS:***

I. ***PATENTS for S3.inc*** **(**http://patft.uspto.gov/netahtml/search-bool.html**: US Patent Trade Mark)**

- Saleh Abdel-hafeez and Nalini Ranjan,"Single Rail Domino Logic for Four-Phase Clocking Scheme", US patent No. 6265899, issue date Oct. 20, 2001.

- Ken-Ming Li and Saleh Abdel-hafeez, "External Power Ring With Multiple Tapings to Reduce IR Drop in Integrated Circuit", US patent No. 20040211982A1, Oct. 28, 2004.

- Saleh Abdel-hafeez and Sarathy P. Sribhashyam, "System and Method for Efficiently Implementing a Double Data Rate Memory Architecture", US patent No. 6356509, March 15, 2002.

II. ***JOURNALS:***

http://ieeexplore.ieee.org/search/freesearchresult.jsp?newsearch=true&queryText=s.+Abdel-hafeez

http://www.springerlink.com/content/?k=Saleh+Abdel-hafeez

A. Saleh Abdel-Hafeez and Behrooz Parhami, "High-Speed and Low-Power Scalable Hamming Weight Comparator Based on a Nonweighted Switched-Capacitor Array," **Journal of Circuits, Systems, and Signal Processing, Springer Publishing Inc.; Accepted 2012; Impact Factor > 0.7.**

B. Saleh Abdel-Hafeez, Ann Gordon-Ross, and Behrooz Parhami "Scalable Digital CMOS Comparator Using a Parallel Prefix Tree", **Journal of IEEE Transactions on Very Large Scale Integration (VLSI) Systems, accepted Sept. 20, 2012. Impact Factor > 0.8**

C. Saleh Abdel-Hafeez and Ann Gordon-Ross, "A Gigahertz Digital CMOS Divide-by-*N* Frequency Divider Based on a State Look-Ahead Structure", **Journal of Circuits, Systems, and Signal Processing, pp.1-24, March 1, 2011. Impact Factor > 0.7**

D. Saleh Abdel-Hafeez and Ann Gordon-Ross, "A Digital CMOS Parallel Counter Architecture Based on State Look-Ahead logic", **Journal of IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, Issue 6, pp. 1023-1034, May 23, 2011. Impact Factor > 0.8**

E. Saleh Abdel-Hafeez, Ann Gordon-Ross, Shadi Harb, Asem Albsoul, and Ahmad Shatnawi, "A Shadow Dynamic Finite State Machine for Branch Prediction: An alternative for the 2-bit Saturating Counter," **An International Journal of Computing and Informatics, Vol. 35, No. 1, Feb. 2010. H Index > 11**

F. Saleh Abdel-Hafeez and Anas Matalkah, "CMOS Eight-Transistor Memory Cell for Low-Dynamic-Power High-speed Embedded SRAMS," **Journal of Circuits, Systems and Computers, Vol. 17, No. 5, pp. 845-863,Oct. 2008. "This work is part from my supervised master thesis to student Anas Matalkah " Impact Factor > 0.2**

G. Saleh Abdel-hafeez and Shadi Harb "A VLSI High Performance Priority Encoder Using Standard CMOS Library", **Journal of IEEE Transactions on Circuits and Systems II, Vol. 53, Number 8, pp. 597-601, Aug. 2006.**
Impact Factor > 0.5

III. ***Conferences:***

A. Saleh abdel-hafeez and Ann Gordon-Ross, "A Comparison-Free Sorting Algorithm", IEEE 11th International SoC Design Conference 2014, Jeju, S. Korea, Nov. 3-7, 2014.

B. Saleh Abdel-Hafeez , Mohammad Shatnawi, and Ann Gordon-Ross, " A DOUBLE DATA RATE 8T-CELL SRAM ARCHITECTURE FOR SYSTEMS-ON-CHIP", IEEE 14Th International Symposium on System-on-Chip 2012, Tampere, Finland, October 11-12, 2012.

C. Saleh Abdel-Hafeez , Shadi M. Harb, and Ken Ming Lee, "On-chip Jitter Measurement Architecture Using A Delay-Locked Loop with Vernier Delay Line, to the order of Giga Hertz", IEEE 18th International conference Mixed Design on Integrated Circuits and Systems 2011.

D. Saleh Abdel-hafeez, " A New High-Speed SAR ADC Architecture," 2010 XIth International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), pp. 1-5, Oct. 3-5, 2010.

E. Saleh Abdel-Hafeez, Shadi M. Harb, William R. Eisenstadt, "High Speed Digital CMOS Divide-by-N Frequency Divider", Symposium on IEEE International Circuits and Systems, (ISCAS) 2008, pp. 592-595, 2008.

F. Saleh Abdel-hafeez and Ahmad Sawalmeh and Sameer Bataineh, "High Performance AES Design Using Pipelining Structure Over GF((24)2)," 2007 IEEE International Conference on Signal Processing and Communication (ICSPC 2007), pp. 716-719, Nov. 24-27 2007. **"This work is part from my supervised master thesis to student Ahmad Sawalmeh "**

G. Saleh Abdel-Hafeez, Shadi M. Harb, William R. Eisenstadt, " Low-Power Content Addressable Memory With Read/Write And Matched Mask Ports," PATMOS 2007, LNCS 4644, pp. 75–85, 2007,Springer-Verlag Berlin Heidelberg 2007

IV. *NEW SUBMITTED JOURNAL PAPERS:*

A. Parhami, S. Abdel-hafeez, A. Damer, "An Efficient Comparison-Based Algorithm for Finding the Median in Small- to Moderate-Size Lists", submitted to IEEE journal of Algorithms

A. S. Abdel-hafeez, B. Parhami, M. Hammory, "A Mixed Analog-Digital Fast Hamming-weight Filtering Circuit Using Switched-capacitor Arrays", Submitted to **Journal of Circuits, Systems, and Signal Processing, Springer Publishing Inc**

V. Ph.D. PUBLICATIONS:

A. S. M. Abdel-hafeez, S. Starks, "A VLSI Modified Architecture for Reduced Symmetric Fuzzy Singleton Set and its applications," in Application and Science of Fuzzy Logic Technology III, S. K. Rogers and D.W. Puck: Editors, Proc. SPIE, vol. 2761, April 1996.

B. S. Abdel-hafeez, S. Starks, and B. Usevitch, "ASIC's Approach Implementation of a Symmetric Triangular Fuzzy Coprocessor and its Application to Adaptive Filtering," accepted at NASA university research center's technical conference on education, aeronautics, space, autonomy, earth, and environment (URC-TC '97), Albuquerque, New Mexico, Feb. 1997.

C. S. M. Abdel-hafeez, S. A. Starks, and J. Ramirez-Angulo, "A Fuzzy Processor Based on Symmetric Triangular Membership Functions," ISSCI, World Automation Congress, Anchorage, Alaska, May 10-14, 1998.

D. S. M. Abdel-hafeez, S. Starks, "A Reduced Symmetric Fuzzy Singleton Set Structure and Its Applications," Memoria Electro'95, XVII Reunion Academica de Ingenieria Electronica, Chihuahua, Mexico, pp. 605-620 (October 1995).

E. S. M. Abdel-hafeez, J. Vega-Pineda, and S. D. Cabrera, VLSI design of an image multi-resolution transform for lossy compression," accepted at NASA university research center's technical conference on education aeronautics, space, autonomy, earth and environment (URC-TC '97), Albuquerque, New Mexico, Feb. 1994.

4) PROFESSIONAL EXPERINCES:

S3.inc, Viatechnology.com, and Altera.com VLSI state-of-the-art Practical Experiences

ALL VLSI circuit projects are achieved in **0.35µ-0.13µ** TSMC/UMC using HSpice, Epic Tools (TimeMill, Powermill, and Path Mill), Arcadia extraction, and Cadence layout tools. In addition, Synopses HDL-Verilog behavioral model is used in order to implement the module structure for Place & Rout and generate all test vectors for testing purposes.

- **Analog Design Blocks:**

I. Design Spacerbias circuit which generates all ref-bias voltages for all Differential input I/O buffer circuits.

II. ***Design and Characterized*** Current switch DAC for our recent product and adjust all necessary sizing as well as work very closely with layout for these new adjustments. Furthermore, enhance the band-gap circuit as well as the reference voltage circuit to provide a stable voltage for all process corners.

III. ***Design and characterized*** a PLL clock synthesis, which run at 800 MHz with 100ps-phase error.

IV. ***Characterized and enhanced*** a Pipeline 8-bit ADC which run at 40Mhz with 1 volt input range and error code correction circuit used for video processor application.

V. ***Design a Charge redistribution*** 8-bit ADC for low power consumption at 100 MHz with 1V input Differential range and 4mv resolution used for 802.11a/b applications. Design the digital logic and Charge Redistribution DAC, and Comparator with 1mv Resolutions at 1ns worst case delay. Used a new approach for digital logic to bring the speed to 100MHz which gives a throughput of 12.5 MHz. In addition, pinpoint the capacitor topology in order to optimize the mismatches and tox gradient. Test chip pass from first time and gives SNR of 46dB at 8 MHz sample rate and 2 MHz input frequency, while the quantization error is +-0.5LSB.

- **Digital Design Blocks:**

I. Designed and IC-Architect L2CACHE/L1CACHE for PC Notebook product at 0.18µ 0.15µ UMC which successfully passed form first time on silicon and run at 200 MHz.
From Initial specification, structured and organized the circuit level Topology and its architecture including all circuit detail, buses, and signals. Instructed and supervised and work very closely with layout Eng. Simulated and design all sizing to meet the Spec. and re-simulate on the post layout and verify the performance on the designed circuit.

II. Designed and participated in I/O 0.18µ and 0.15µ UMC; Currently, the leader on 0.15µ I/O UMC.
Designed and Structured Input buffer for AGP4X, AGP2X, PCI, and SSTL. In addition, designed the legs structure driver for SSTL, AGP4X, AGP2X, and PCI to meet all DC Spec. and all Trans. Spec.; Furthermore, pinpointed the DDR simulations for Output and input as well as all AGP4X/AGP2X signal integrity. The driver is designed to meet 5v-tolerant. Furthermore, designed the pre-driver to select appropriate legs codes structure with minimum Crowbar current and low transient currents. Work very closely with layout Eng.

III. Designed and pinpointed the compensation Pad that selects appropriate codes in pre-driver for different process corners.

IV. Designed and Characterized/Enhanced several SRAM Blocks, such as 64-address X 256-bit, 244X128, etc. with many different configurations at 200-300 MHz.

5) Teaching Courses

- **Santa Clara University (USA):**

1. **Digital VLSI; Book: Fundamental of MOS Digital Integrated Circuits, by John P. Uyemura**
2. **Analog VLSI; Book: Design of Analog Integrated Circuits, by Behzad Razavi**

- **Jordan University of Science and Technology:**

1. Java Programming
2. Computer Graphics
3. Computer Organization
4. Computer Design Arithmetic
5. Digital VLSI
6. Advance VLSI for graduate student
7. Computer Design language
8. Computer assembly language (68K, 8086, MIPS, and ARM)
9. Unix operating system
10. Operating Systems; Book: Operating Systems Design and Implementation, by Andrew S. Tanenbaum and Albert S. Woodhull
11. Microprocessor II (68008, 8086)
12. Computer Architecture I
13. Advance Computer Architecture II
14. FPGA and application for Embedded System
15. Numerical analysis
16. Seminar for graduate students
17. Data Communications

- **Bahrain University (Bahrain)**

1. System Programming (Computer Systems: A Programmer's Perspective) by Randal E. Bryant and David R. O'Hallaron
2. VLSI Design
3. Computer Architecture I
4. PCs Maintenance and Troubleshooting
5. Microprocessor (Intel 80x86/85)

6) *Title of Supervised Master Thesis (attach abstract):* Average enrolled students for graduate program per year is around five students and there is no Ph.D. program

I. VLSI Design—

1. CMOS EIGHT-TRANSISTOR MEMORY CELL FOR LOW-POWER HIGH-SPEED EMBEDDED SRAM, JAN. 2006

Student: Anas Matalkah Main Advisor: Dr. Saleh Abdel-hafeez

2. Double Data Rate Synchronization Using Delay-Locked Loop to the Order of Nano-second, 2011

Student: Laith Waleed Shahab Main Advisor: Dr. Saleh Abdel-hafeez

3. System and Method For Efficiency Implementing a Double Line Memory Architecture Using Nanotechnology

Student: Mohammad Khair Shatnawi Main Advisor: Dr. Saleh Abdel-hafeez

II. Computer Architecture —

1. DYNAMIC BRANCH PREDICTION SCHEMES AND PERFORMANCES, AUG. 2005

Student: Shatha Alhasan Main Advisor: Dr. Saleh Abdel-hafeez

III. VLSI Design for Network Security

1. HARDWARE DESIGN OF AES S-BOX USING PIPELINING STRUCTURE OVER GF($(2^4)^2$), 2007

Student: Ahmad Sawalmeh Main Advisor: Dr. Saleh Abdel-hafeez

IV. Computer Vision—

1. DETECTION OF BREAST CANCER IN THE JPEG2000 DOMAIN, 2005

Student: Nehal Zubaidi Committee Member: Dr. Saleh Abdel-hafeez

7) SELECTED GRADUATION PROJECTS FOR YEAR 2004-2010

1. Braille Training Kit
2. FPGA IMPLEMENTATION FOR VGA CONTROLLER:
3. FPGA IMPLEMENTATION FOR REAL-TIME PC MONITOR AND KEYBOARD DISPLAY
4. IMPLEMENTATION OF ROBOT CAR CONTROLLER USING FPGA TECHNOLOGY
5. HOME AUTOMATION VIA BLUETOOTH
6. COURSE SCHEDULING MANAGEMENT
7. MULTIPURPOSE SHARED APPLICATION ENVIRONMENT
8. Android Applications for English learning pronunciations and recognition
9. Automatic voice recognition for helping blind eye-sighted people
10. Tracing sun PV mirror using fuzzy controller
11. Automatic detection of screw threading using computer vision concept
12. Game programing using FPGA kit